ABSTRACT
This article studies on the design of sliding mode controller (SMC) plus fuzzy logic controller (FLC) for the performance analysis of negative output elementary super lift Luo converter (NOESLLC) operated in discontinuous conduction mode (DCM). The main benefits of NOESLLC are high voltage transfer gain, high efficiency, and reduced inductor current and capacitor voltage ripples. The main problem when operating the NOESLLC in continuous conduction mode (CCM) is having a right half pole zero (RHPZ) in the transfer function (control signal to output). But in DCM the NOESLLC has no RHPZ and also have other merits such as high dynamic response, avoidance of reverse recovery crisis of diode, suitability for partial/light load conditions and improved stability. Owing to time-varying switching characteristics of NOESLLC in DCM, its dynamic performance is alienated in many situations. With the intention of increasing the dynamic performance and the output voltage regulation of NOESLLC in DCM, SMC plus FLC is developed. Here, the SMC is presented in the inner loop for controlling the inductor current and the FLC is used in the outer loop for regulating the output voltage. The SMC parameters are designed with help of the state space average model of NOESLLC, whereas the FLC rules are designed based on knowledge of converter performance. The performance of complete model is verified at various operating regions by developing the MATLAB/Simulink model.

KEY WORDS: DC-DC Converter, Negative Output Elementary Super Lift Luo Converter (NOESLLC), Discontinuous Conduction Mode (DCM), Sliding Mode Controller(SMC), Fuzzy Logic Controller(FLC), State Space Averaging, Proportional-Integral Controller(PIC).

INTRODUCTION
The negative output elementary boost converter (NOESLLC) is a one of the attractive DC-DC converter topology that gives a controlled negative output D.C voltage from a positive D.C input voltage. The main significance of this converter has a high-quality voltage transfer gain (in geometric progression), an excellent efficiency, a suppressed inductor/capacitor ripples in comparison with conventional DC-DC converters [1-2]. It is more fit for power supply in battery control models applications such as digital camera, lap-top computers, thin-film-transistor liquid-crystal display (TFT LCD), computer mother board, mobiles etc. For all these applications, it is significant to expand the life time of battery. Therefore, the efficiency is critical even converters operate at light load or no load conditions. The NOESLLC can be operated in two modes. First option is the continuous conduction mode (CCM), the inductor current of the converter never falls to zero, where a right half plane zero (RHPZ) is obligatory. This makes the system complex and creates stability issues and hence it is not appropriate to light load applications. Secondly, when the same converter operates in the discontinuous conduction mode (DCM) does not have RHPZ, improves system stability, avoids the reverse recovery problem of the diode and also becomes more suitable for low power application [3-4]. The control methodology for NOESLLC operated in DCM is required to be examined before suggesting it to specific applications. The performance analysis of various DC-DC converters in DCM has been reported [5-12]. The mathematical modeling of various DC-DC converters has been reported [13-16]. Among these modeling methods, the state space averaging method has been most famous modeling approaches for DC-DC converters topologies. The classical linear controller methodology for various DC-DC converters has been well executed [16-17]. Hitherto, these classical controllers are very sensitive to circuit parameter variations, exhibit poor stability during large line and load variations etc.

The conquest of non-linear controller lies in performing superiority against these problems as dc-dc converters are intrinsically variable structure systems (VSS). The controller of NOESLLC must cope with their intrinsic nonlinearity and wide input voltage and load variations, ensuring stability in any operating condition while providing fast transient and improved dynamic responses. Essentially, the SMC utilizes a high-speed switching control law to drive the nonlinear state trajectory onto a specified surface in the state space, called the sliding or switching surface, and to maintain it on this surface for all subsequent time [18-20]. Claim of SMC at variety of sliding surfaces for dc-dc converters activated in CCM has been well addressed in the past [21-22]. The order reduction based SMC for CCM operation in Cuk’ dc-dc converter has been dealt [23]. Fixed switching frequency SMC for NOESLLC operated in CCM has been well executed [24]. In the above cases, the SMCs offer several merits over the linear proportional integral controller (PIC) or proportional integral derivative controller (PIDC); they provide stability even for large line and load variations, robustness, good dynamic response and simplicity in implementation. The fuzzy logic controller (FLC) based SMC and PIC for dc-dc converters operated in CCM has been reported [25-26]. However, fuzzy logic systems demand a time-consuming trial-and-error tuning method and also the control design is purely heuristic. The conventional SMCs are enforcing the system phase trajectory along with ideal sliding surface at infinite frequency. This is undesirable, as high operating switching frequency will result in extravagant switching losses, inductor loss and electromagnetic interference (EMI) noise.
problems. To overcome these problems, hysteresis band with the boundary conditions are commonly employed. The variable switching frequency based SMC for CCM operation of Luo converter presented in past decades [27-28]. The DCM operation of buck, buck boost and fly back converters using hyper plane SMC has been reported [29]. However, the designed SMC has complex structure, need more number of sensors, and more control circuit cost. From the above literatures, it is clearly observed that design of control methodology for NOESLLC in DCM has not been reported.

In this article, it is proposed to design a simple sliding surface based variable frequency SMC plus FLC for NOESLLC to function in DCM. The state-space average model for NOESLLC in DCM is derived at first and then SMC plus FLC is designed. The performance of NOESLLC in DCM with SMC plus FLC is verified at different operating regions through proper selection of the controller parameters over SMC plus PIC. The tuning of PIC parameters are obtained by using Ziegler Nichol’s tuning method. The organization of this paper is as follows. Section 2 presents the circuit operation and state-space average modeling of the NOESLLC in DCM. The systematic step by step design procedure of SMC plus FLC/PIC for the NOESLLC is presented in section 3. The simulation results of the NOESLLC using SMC plus FLC/PIC at the various operating regions are discussed in sections 4. The major conclusions are listed in section 5.

2. ANALYSIS OF DCM OPERATION OF NOESLLC

The power circuit of NOESLLC is shown in Fig.1 (a), and the state/mode 1 (switch Q ON) and 2 (Q OFF) operations are respectively presented in Fig.1(b) and Fig.1(c). The state 3 (DCM) is indicated in Fig.1 (d) while the inductor current is pictured in Fig.1 (e). The capacitor voltage can be assumed as constant as the common selection of capacitor is much higher than the minimum demanded value. In the Fig. 1(e), T is the switching time period and d is the duty cycle. During the period \([d+d'] T \leq t \leq T\], the current through the inductor is zero; switch is in OFF state, and diodes D1 and D2 are in OFF state as shown in Fig.1(d) [1-3]. From the Fig.1 (e), the condition of DCM is expressed as

\[ d + d' < 1 \tag{1} \]

During \(0 \leq t \leq d T\), \(i_{L1}\) increases with slope \(V_m / L_1\) and during \(dT \leq t \leq (d + d')T\), \(i_{L1}\) decreases with slope \(- (V_o - V_m) / L_1\). Hence,

\[ \Delta i_{L1} = \frac{V_m}{L_1}dT = \frac{V_o - V_m}{L_1}d'T \tag{2} \]

The above equation (2) can be simplified as

\[ V_m d = (V_o - V_m) d' \tag{3} \]

In the steady state condition, the average capacitor current is zero. Considering the current in \(C_o\) in Fig. 1. (b), (c) and (d), the following relations are obtained;

\[ d'T = \left( \frac{1}{2} \Delta i_{L1} - I_o \right) = dTI_o + (1-dd')TI_o = (1-d')TI_o \tag{4} \]

Using \(\Delta i_{L1} = \frac{V_m}{L_1}dT\) from (2), and substituting \(I_o = \frac{V_o}{R}\) and \(T = \frac{1}{f}\) in (4) results in (5)
\[
\frac{1}{2} V_{in} \frac{d^2}{dL_1} = \frac{V_o}{R_o}
\]  
(5)

Combining (3) and (5) becomes
\[
d^2 = \frac{dV_{in}}{V_o} \frac{2fL_1V_o}{V_{in}} \frac{dR}{V_{in}}
\]  
(6)

Next, defining the voltage transfer gain \( G = \frac{V_o}{V_{in}} \) in equation (6) gives
\[
d^2 = \frac{d}{G-1} \frac{2fL_1G}{dR}
\]  
(7)

Therefore,
\[
G^2 - G \frac{d^2 R}{2L_1f} = 0
\]  
(8)

Solving the equation (8), expresses the voltage transfer gain as follows.
\[
G = \frac{1}{2} \left( 1 + \sqrt{1 + 2d^2 \frac{R}{L_1f}} \right)
\]  
(9)

2.1 Condition of DCM and validation

The condition of DCM is expressed in (1). Substitution of (7) in (1) gives,
\[
d^2 \frac{d}{G-1} < 1 \quad \Rightarrow \quad \frac{d}{G-1} < 1 - d \quad \Rightarrow \quad G-1 > \frac{d}{1-d} \quad \Rightarrow \quad G > 1 \frac{1}{1-d}
\]  
(10)

Substitution of (9) into (10) engraves as (11)
\[
\left( 1 + \sqrt{1 + 2d^2 \frac{R}{L_1f}} \right) > \frac{2}{1-d} \quad \Rightarrow \quad 1 + 2d^2 \frac{R}{L_1f} > \left( \frac{2}{1-d} \right)^2 = \left( \frac{1+d}{1-d} \right)^2
\]  
(11)

The equation (11) is the condition for DCM in the NOESLLC. This equation can be verified from the variation ratio of inductor current in CCM.
\[
\xi = \frac{\Delta i_{L1}}{i_{L1}} = d(1-d)^2 \frac{R}{2fL_1}
\]  
(12)

Where, \( \xi < 1 \) in the CCM and \( \xi > 1 \) in the DCM. Then the DCM condition is
\[
d(1-d)^2 \frac{R}{2fL_1} > 1 \quad \Rightarrow \quad \frac{R}{L_1f} > \frac{2}{d(1-d)^2}
\]  
(13)

The equation (13) agrees with equation (11)
\[
\frac{R}{L_1f} < g(d)
\]  
(14)

Where, \( g(d) = \frac{d(1-d)^2}{2} \) for which \( 0 < d < 1 \). The maximum range of \( g(d) \) is derived as
\[
g'(d) = \frac{1}{2} (3d^2 - 4d + 1) = 0 \quad \Rightarrow \quad d = \frac{1}{3} \quad \Rightarrow \quad g_{max}(d) = g\left( \frac{1}{3} \right)
\]  
(15)

\[
\frac{2}{27}
\]

Fig. 2. Graphical analysis of equation (15).
Therefore, as the model of NOESLLC may be reached as expressed by (16).

\[
\Delta V_o = \frac{\Delta Q}{C_o} = \frac{I_o dT + I_r (1 - d - d') T}{C_o} = \frac{I_r (1 - d') T}{R f C_o} = \frac{V_o (1 - d')}{R f C_o}
\]

(16)

Where,

\[1 - d' = \frac{\Delta Q}{C_o} = 1 - \frac{2 L_r f G}{d R} = 1 - \frac{L_r f}{1 + 2 d^2 \frac{R}{L_r f}}\]

2.2 State space averaging modeling of NOESLLC in DCM

In mode 1 operation, when the switch Q is ON, the diode D1 performs. The capacitor C1 is charged by supply voltage, \(V_{in}\). The diode D1 conducts only for short duration of time period and this capacitor voltage is assumed as a firm value. The current through the inductor \(L1\), \(i_{L1}\) rises with \(V_{in}\). The output capacitor, \(C_o\), offers the energy to the output load. The equivalent circuit of NOESLLC in mode 1 operation is shown in Fig. 1(b). The state space equation can be scratched as follows.

\[
\begin{align*}
L \frac{d i_{L1}}{dt} &= V_{in} \\
C_o \frac{dV_o}{dt} &= -\frac{V_o}{R}
\end{align*}
\]

(17)

Switch ON

During the mode 2 operation, switch Q is in OFF state, diode D2 is ON and therefore, the inductor current decays with the \(C_1\) voltage \((V_o - V_{in})\) while supplying the energy to \(C_o\) and load. The equivalent circuit of NOESLLC in mode 2 is shown in Fig.1(c). The state space equation can be marked as (18)

\[
\begin{align*}
L \frac{d i_{L1}}{dt} &= V_{in} - V_o \\
C_o \frac{dV_o}{dt} &= i_{L1} - \frac{V_o}{R}
\end{align*}
\]

(18)

Switch OFF

Using the capacitor charge balance rule on \(C_1\), the equation (3) for whole switching time period can be rewritten. Where, 't' is the status of the switch (d=1 when the switch is ON, and d=0 when the switch is OFF).

\[
d C_1 \frac{d V_{cl}}{dt} + (1 - d) i_{L1} = 0
\]

(19)

During the DCM operation (refer the Fig. 1 (d)), the state space equation can be expressed as

\[
\begin{align*}
\frac{d i_{L1}}{dt} &= 0 \\
\frac{V_o}{R} + C_o \frac{dV_o}{dt} &= 0
\end{align*}
\]

(20)

To proceed further it is required to choose the state space variables. The inductor current \(i_{L1}\) and output voltage \(V_o\) are selected as state variables respectively as \(x_1\) and \(x_2\). Using (17), (18), (19) and (20), the state-space average modeling of the NOESLLC may be reached as expressed by (21).

\[
\begin{bmatrix}
i_{L1} \\
V_o
\end{bmatrix} =
\begin{bmatrix}
0 & -\frac{d'}{L_1} \\
\frac{d'}{C_o} - \frac{1}{RC_o}
\end{bmatrix}
\begin{bmatrix}
i_{L1} \\
V_o
\end{bmatrix}
+ \begin{bmatrix}
\frac{d + d'}{L_1} \\
0
\end{bmatrix} V_{in}
\]

(21)

As the model of NOESLLC involves only one inductor and the dimension of 'x' is also two, the modification matrix denoted by W is simply given as (22).

\[
W = \begin{bmatrix}
1 & 0 \\
0 & 1
\end{bmatrix}
\]

(22)

Therefore, the modified averaged model of NOESLLC in DCM can be written as (23)
\[
\begin{bmatrix}
\dot{i}_{L1} \\
\dot{v}_o
\end{bmatrix}
= \begin{bmatrix}
0 & -\frac{d'}{L_1} \\
\frac{d'}{C_o} - \frac{1}{RC_o}
\end{bmatrix}
W
\begin{bmatrix}
i_{L1} \\
v_o
\end{bmatrix}
+ \begin{bmatrix}
\frac{d+d'}{L_1} \\
0
\end{bmatrix}
V_{in}
\]

\[
\begin{bmatrix}
\dot{i}_{L1} \\
\dot{v}_o
\end{bmatrix}
= \begin{bmatrix}
0 & -\frac{d'}{L_1} \\
\frac{d'}{C_o(d+d')} - \frac{1}{RC_o}
\end{bmatrix}
\begin{bmatrix}
i_{L1} \\
v_o
\end{bmatrix}
+ \begin{bmatrix}
\frac{d+d'}{L_1} \\
0
\end{bmatrix}
V_{in}
\]

where, \( A = \begin{bmatrix}
0 & -\frac{d'}{L_1} \\
\frac{d'}{C_o(d+d')} - \frac{1}{RC_o}
\end{bmatrix} \), \( B = \begin{bmatrix}
\frac{d+d'}{L_1} \\
0
\end{bmatrix} \), \( C = [0 \ 1] \), \( D = 0 \) \( (23) \)

2.3 Design of NOESLLC circuit elements in DCM

Using the above model equations, the detailed design and specifications of NOESLLC circuit is obtained and recorded in Table 1.

The design specifications are substituted in equation (23) and after using the phase-variable transformation, the system matrices become,

\[
A = \begin{bmatrix}
0 & -4666.67 \\
23281.5 & 109.1
\end{bmatrix}, \quad B = \begin{bmatrix}
0 \\
1
\end{bmatrix} \quad (24)
\]

Table 1. Specifications of the NOESLLC (Application in Digital Camera)

<table>
<thead>
<tr>
<th>Parameters name</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>( V_{in} )</td>
<td>10V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>( V_o )</td>
<td>-19.6V</td>
</tr>
<tr>
<td>Inductor</td>
<td>( L_i )</td>
<td>45 ( \mu )H</td>
</tr>
<tr>
<td>Capacitors</td>
<td>( C_i, C_o )</td>
<td>4.7 ( \mu )F, 22 ( \mu )F</td>
</tr>
<tr>
<td>Nominal switching frequency</td>
<td>( f )</td>
<td>100kHz</td>
</tr>
<tr>
<td>Load resistance</td>
<td>( R )</td>
<td>416.16 ( \Omega )</td>
</tr>
<tr>
<td>Average input current</td>
<td>( I_{in} )</td>
<td>0.11A</td>
</tr>
<tr>
<td>Efficiency</td>
<td>( \eta )</td>
<td>82.5%</td>
</tr>
<tr>
<td>Average output current</td>
<td>( I_o )</td>
<td>-0.047 A</td>
</tr>
<tr>
<td>Duty ratio</td>
<td>( d )</td>
<td>0.2</td>
</tr>
<tr>
<td></td>
<td>( d' )</td>
<td>0.21</td>
</tr>
<tr>
<td>Peak to Peak Capacitor Ripple</td>
<td>( \Delta V_o )</td>
<td>-0.01V</td>
</tr>
</tbody>
</table>

3. DESIGN OF CONTROL METHODOLOGY
The main aim of this section is to discuss about the controller for the NOESLLC in DCM operation. The proposed system of arrangement of SMC plus FLC/PIC applicable to the NOESLLC is depicted in Fig. 3 (a). The designed controller is split into two loops namely, an inner current loop with SMC to guide the inductor current and an outer voltage control loop utilizing the FLC. The position of FLC is replaced with a PIC to perform the comparative study. The input to the FLC/PIC is the output voltage error while the controller establishes the mean value reference inductor current for inner loop. The inputs to the SMC are output voltage error, \( e_1 \) and the inductor current error \( e_2 \). The output of SMC is the regulating signal, which in turn sets the new duty ratio of the switching pulse for driving the power MOSFET switches of the NOESLLC in DCM.

3.1 Design of SMC

Phase variable transformation technique is used to imply the NOESLLC in DCM. Keeping the sliding surface \( \sigma(e,t) \), the model of the NOESLLC (DCM) in phase-variable form is expressed as in equation (25).

\[
\dot{X} = AX + Bu
\]  

(25)

Where,
\[
A = \begin{bmatrix} 0 & -4666.67 \\ 23281.5 & 109.1 \end{bmatrix}, \quad B = \begin{bmatrix} 0 \\ 1 \end{bmatrix}
\]  

(26)

Let, the 'H' be the vector which contains dynamic variables, \( X \) be the original state variables and \( e \) be the error vector.

\[
H = \begin{bmatrix} h_1 \\ h_2 \end{bmatrix}^T, \quad X = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}^T, \quad e = \begin{bmatrix} e_1 \\ e_2 \end{bmatrix}^T
\]  

Having considered the actual state variables as \( x_1 = i_{L1} \) and \( x_2 = V_o = V_{co} \), the dynamic reference variables are \( h_1 = i_{L1ref} \), \( h_2 = V_{oref} \). The error values \( e_1 \) and \( e_2 \) are expressed as (27)

\[
e_1 = \begin{bmatrix} h_1 - x_1 \\ i_{L1ref} - i_{L1} \end{bmatrix}, \quad e_2 = \begin{bmatrix} h_2 - x_2 \\ V_{oref} - V_o \end{bmatrix}
\]  

(27)

The switching function of the converter is expressed as sliding surface.

\[
\sigma = N_1 e_1 + N_2 e_2
\]  

(28)

Where, \( e_1 \) and \( e_2 \) are the errors of the converter and it can be written as equation (29)

\[
e_1 = \begin{bmatrix} i_{L1ref} - i_{L1} \\ V_{oref} - V_o \end{bmatrix}, \quad e_2 = \begin{bmatrix} V_{oref} - V_o \end{bmatrix}
\]  

(29)

The tracking vector of the NOESLLC is written as equation (30)

\[
\sigma(e,t) = [N][e]
\]  

(30)

The error vector in the sliding surface is always to maintain the condition \( \sigma(e,t) = 0 \) (for all the time) with the controller co-efficient vectors, \( N = [N_1, N_2] \) and \( N_1, N_2 > 0 \).

\[
\dot{\sigma}(e,t) = [N][e] = 0
\]  

(31)

The sliding surface of the second order converter is reduced into get the first order model through the differential equations and it can be written as equation (32)

\[
\dot{e} = \ddot{H} - \dot{X} \\
\quad e = \ddot{H} - AX + Bu
\]  

(32)
Substituting $X = H - e$ in (32) and Filippov’s equivalent switch control $u_{eq}$ that pledges the $\dot{e}(e,t) = 0$ gives

$$\dot{e} = Ne = \left[N \left[ \dot{H} - AH + Ae - Bu_{eq} \right] \right] = 0 \tag{33}$$

The converter control signal is estimated using the equation (33) and it will be written as equation (34)

$$u_{eq} = \left[ NB \right]^{-1} N \left[ \dot{H} - AH + Ae \right] \tag{34}$$

By substituting equation (34) in equation (32)

$$\dot{e} = \left[ \dot{H} - AH + Ae - B (NB)^{-1} N \dot{H} - AH + Ae \right]$$

$$\dot{e} = \left[ I - B (NB)^{-1} N \dot{H} - AH + Ae \right] \tag{35}$$

Substituting $\dot{H} - AH = 0$ (invariance conditions) in equation (36) the expression has been simplified as

$$\dot{e} = \left[ I - B (NB)^{-1} N \right] Ae = A_{eq} e \tag{37}$$

If $(NB)^{-1}$ exists, the vector $N$ is derived by choosing the eigen values of $A_{eq}$ such that it guarantees the asymptotic convergence of error to zero at the desired value. The matrix $A_{eq}$ is selected to satisfy equation (37) and it is expressed as

$$A_{eq} = \begin{bmatrix} -6.6 & 0 \\ 0 & -6.6 \end{bmatrix} \tag{38}$$

The values of matrix $N$ is then found using equation (37) as

$$N = \begin{bmatrix} N_1 & N_2 \end{bmatrix} = \begin{bmatrix} 1 & 2.06 \end{bmatrix} \tag{39}$$

Thus, the sliding manifold $\sigma$ is given by

$$\sigma = N_1 e_1 + N_2 e_2 \tag{40}$$

Equation (40) marks that if the NOESLLC works in stable mode (when $\sigma = 0$, stability condition), the dynamics of errors $e_1$ and $e_2$ are to decay exponentially to zero with a time ratio of $N_1/N_2$. Even as in the step transient’s period, the NOESLLC in DCM is in reaching mode, and so for this $N_1$ and $N_2$ are evaluated to be 1 and 2.06, respectively. In addition, the equation (28) describes the error action under SMC. Once the sliding surface $\sigma(e, t) = N e$ is designed then the control law for hitting condition is defined as

$$u = M \text{sgn}(\sigma)x_2$$

$$= U x_2 \tag{41}$$

Where,

$$U = \begin{cases} 1 \quad \text{for } \sigma > \delta \\ 0 \quad \text{for } \sigma < \delta \end{cases}$$

($U = 1$ when the switch is the conduction subinterval, and $U = 0$ when the diode is the conduction subinterval).

In this case, hysteresis bandwidth $\delta = 0.05$ is selected by trial and error iterative method (based on the system performance). Equation (41) is used to derive the gate pulse to drive power MOSFETs of converter, which in turn control dc output voltage, steady state error and inductor current. In this study, $M$ is constant number and equal to unity so that $\sigma \sigma < 0$ (existence condition is fulfilled). The reaching condition guarantees that the tracking error phase trajectory is asymptotically involved to $\sigma = 0$ (stability condition). It is shown that the (41) does not depend on the working regions, system parameters and limited disturbances. This is achieved as long as the control input $u$ is more enough to maintain the converter subsystem in sliding mode.

$$\sigma(X) = N^T X_i + N_2 X_2 \tag{42}$$

Where, $N^T = [1, N_2]$ is the vector of sliding surface coefficients which correspond to $K$ in equation (33)

$$\dot{\sigma}(X) = \begin{cases} \dot{N}^T X_i + N^T B U^+ + C^T D_e, & \text{for } \sigma(X) > 0 \\ \dot{N}^T X_i + N^T B U^+ + C^T D_e, & \text{for } \sigma(X) < 0 \end{cases} \tag{43}$$

Then, substituting the values of $A$, $B$, and $N$, the above equation can be expressed by

$$\sigma(X_i) = 23281.5 N_2 X_i - 4666.67 N_1 X_i + 109.1 N_2 X_2$$

$$\sigma(X_2) = 23281.5 N_2 X_1 - 4666.67 N_1 X_1 + 109.1 N_2 X_2 + N_2 \tag{44}$$

Equations $\sigma_1(X) = 0$ and $\sigma_2(X) = 0$ define two lines in the state plane with the same slope flowing through the origin. These equations signify the sliding surface for switch ON/OFF states regions. From this phase trajectory, it is evidently observed that the suitable value of $N_2$ controls the dynamic response of the system. Once the phase trajectory is on top of the sliding surface, the switch is turned off ($U=0$) and when the phase trajectory is below the sliding surface, the switch is turned on ($U=1$). Also, from the Fig. 3 (b), it is
understood that overshoots in the phase trajectory of the converter using the SMC plus FLC is small when compared to the SMC plus PIC.

3.2 Design of PIC
A PIC is chosen for providing the good output voltage regulation for NOESLLC. In this case, the PIC output sets the average reference inductor current for inner current loop. The PIC parameters, proportional gain ($K_p$) and integral time ($T_i$), are evaluated using Zeigler–Nichols tuning method [15-18]. After the tuning the controller using this method, the NOESLLC is providing a sustained oscillation with ultimate gain for stability as $K_{cr}=0.2$ and their corresponding ultimate period $P_{cr}=0.2s$. Using this method the values of $K_p=K_{cr}/2=0.1$ and integral time is determined as $T_i=P_{cr}/2=0.1s$.

3.3 Development of FLC
In this article, the FLC is used as a outer loop to regulate the output voltage in DCM. The FLC inputs and output are shown in Fig. 4 (a) to (c). The output voltage error ($e$) and its change in voltage error ($ce$) are applied as a input to the FLC and the output is the inductor current reference ($o$). For suitability, the arithmetic ranges of the inputs/output of the FLC can be normalized and expressed as pursues: $e=-0.1 -0.06 -0.02 0 0.02 0.06 0.1$, $ce=-0.4 -0.24 -0.08 0 0.08 0.24 0.4$ and $o=-3 -2 -1 0 1 2 3 4.067 4.033 4.03 4.067 5$. Its related fuzzy sets are [NB, NM, NS, Z, PS, PM, PB], where, NB is negative big, NM is negative medium, NS is negative small, Z is zero, PS is positive small, PM is positive medium and PB is positive big. The membership functions of the $e$, $ce$, and $o$ are marked in Fig. 4. The assortment of FLC rules completely depends on the performance characteristics of the NOESLLC. In this article, 49 rules are structured (refer the Table 2). Subsequently, the weighted average method (defuzzification) is utilized to complete the FLC design.

![Fig. 4 Membership’s functions of FLC, (a) error (e), (b) change in error (ce), and (c) output (o).](image)

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Table 2. Fuzzy Rule for NOESLLC in DCM.
4. RESULTS AND DISCUSSION
This section deals about the simulation results of NOESLLC in DCM using SMC plus FLC/PIC. The NOESLLC in DCM performance is verified at various conditions viz. start-up transient, line variation, load variation and also circuit components variations.

4.1 Start-up region
Fig.6 shows the simulated output voltage results of NOESLLC in DCM using the SMC plus FLC and SMC plus PIC in start-up transient region with nominal input voltage. From this figure, it is evident that the output voltage has null overshoots, settling time of 0.5ms, and little steady state error around -0.1V using SMC plus FLC, but the same converter with SMC plus PIC has produced peak overshoots of -0.5V and settling time of 3.5ms during start-up transient region.

![Fig.6. Start-up overshoots in output voltage responses with rated input voltage.](image)

4.2 Line Variation

![Fig.7. Output voltage and inductor current of NOESLLC in DCM using SMC plus FLC and SMC plus PIC for input step change from 10V to 13 V at time of 0.05s with R = 416.6Ω. (a) Simulation, (b) Zoomed simulation output voltage, and (c) Inductor current.](image)
Fig. 7 shows the simulated output voltage and inductor current results of NOESLLC in DCM using the SMC plus FLC and SMC plus PIC for input voltage change from 10V to 13V at time of 0.05s with R = 416.6Ω. From the Figs. 7 (a), (b), it is clearly proved that the output voltage of the NOESLLC in DCM has null overshoots, zero settling time, and steady state error around -0.1V using SMC plus FLC, whereas with SMC plus PIC has produced peak overshoots of ~0.1V and settling time of 0.005s during line disturbance region. Fig. 7 (c) indicates that the inductor current has produced null overshoots and settling time in line variation.

Fig. 8 shows the simulated output voltage and inductor current results of NOESLLC in DCM using the SMC plus FLC and SMC plus PIC for input voltage change from 10V to 07V at time of 0.05s with R = 416.6Ω.

From the Figs. 8 (a), (b), it is clearly focused that the output voltage of the NOESLLC in DCM has null overshoots, zero settling time, and steady state error around -0.1V using SMC plus FLC, while the NOESLLC in DCM with SMC plus PIC has produced peak overshoots of ~0.5V and settling time of 0.005s during line disturbance region. Fig. 8 (c) indicates the inductor current of NOESLLC in DCM with controllers has produced null overshoots and settling time in line variation.

4.3 Load variation
Fig. 9. Output voltage, output current, and inductor current using SMC plus FLC and SMC plus PIC for load resistance change from 416.6Ω to 316.6Ω at time of 0.05s with input voltage of 10V, (a) Simulation, (b) Zoomed simulation output voltage, and (c) Inductor current.

Fig. 9 shows the simulated output voltage, output current, and inductor current using the SMC plus FLC and SMC plus PIC for load resistance change 416.6Ω to 316.6Ω at time of 0.05s with input voltage of 10V. The results show that the output voltage of the NOESLLC in DCM has null overshoots, zero settling time, and steady state error around -0.1V using SMC plus FLC, while the NOESLLC in DCM with SMC plus PIC has produced peak overshoots of -0.07V and settling time of 0.005s during load disturbance region. Fig. 9(c) indicates the perfect settlement of inductor current in load variation.

Fig. 10 shows the simulated output voltage, output current, and inductor current results with SMC plus FLC and SMC plus PIC for load resistance change 416.6Ω to 516.6Ω at time of 0.05s with input voltage of 10V. From the Figs. 10 (a), (b), it is understood that the output voltage of the NOESLLC in DCM has null overshoots, zero settling time, and steady state error around -0.1V using SMC plus FLC, while the NOESLLC in DCM with SMC plus PIC has produced peak overshoots of -0.07V and settling time of 0.005s during load disturbance region.

Fig. 10. Output voltage, output current, and inductor current using SMC plus FLC and SMC plus PIC for load resistance change from 416.6Ω to 516.6Ω at time of 0.05s with input voltage of 10V (a) Simulation (b) Inductor current
4.4 Steady state region

Fig. 11. Simulated response of output voltage, inductor current \( i_{L1} \) and gate pulse in steady state condition using SMC plus FLC

Fig. 11 shows the simulation response of instantaneous output voltage, gate pulse and the inductor current of the NOESLLC in DCM during steady state region using a SMC plus FLC. It is evident from the figure that the output voltage ripple is very small about -0.015V and the peak to peak inductor ripple current is 0.5 A.

4.5 Circuit Components variations

Fig. 12. Circuit components variations and performance of NOESLLC in DCM, (a) Simulation response of output voltage when inductor variation from 45\( \mu \)H to 90\( \mu \)H using both controller schemes (b) Simulation response of output voltage when inductor variation from 22\( \mu \)F to 32\( \mu \)F using both controller schemes.

Fig. 12 (a) and (b) shows simulated results of output voltage of NOESLLC in DCM using both controllers in circuit components variation (i.e. inductor vary from 45\( \mu \)H to 90\( \mu \)H and output capacitor vary from 22\( \mu \)F to 32\( \mu \)F). From these disturbances, the results are shown that the output voltage of this converter in DCM is not affected.

Fig. 13. Simulation responses of average input current, current, input voltage, output current, output voltage and efficiency.

Fig. 13 shows that the simulation results of average input current, inductor current, input voltage, output current, output voltage and efficiency of NOESLLC in DCM using SMC plus FLC. From these results, it is found that the numerical values of average input current of 0.11A, inductor current of 0.5A, input voltage of 10V, output
5. CONCLUSIONS

In this article, the analysis, design, inductor current and output voltage regulation of the NOESLLC operated in DCM using a variable frequency based SMC plus FLC/PIC has been successfully implemented. The advantages of designed controller over a linear PIC are robust to huge changes on line, and load, purges the steady state error, unproblematic implementation, and good quality output response even though the circuit parameter variations. Simulations results are accessible to represent the efficacy of designed SMC plus FLC for the NOESLLC operated in DCM in rapid dynamic response, improved stability, adept regulated output voltage, non-disturbed output voltage under the circuit component disparities, small steady state error and start-up responses etc. It is, so, appropriate for any unvarying low power battery source operated real-world commercial applications such as different medical equipments, digital camera, lap-top computers, TFT-LCD bias supplies, computer mother board, mobile phones and telecom.

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