CONTROL OF CURRENT IN PARALLELED CONNECTED CONVERTERS FOR STANDALONE PHOTOVOLTAIC SYSTEM

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ABSTRACT

This paper proposes a new scheme for avoiding sharing of load current in two or more parallel connected converters for standalone photovoltaic system. Because of different circuit parameters in parallel connected converters, no equal sharing of load current takes place. In order to achieve correct sharing of load current new current sharing scheme is proposed. The proposed scheme doesn’t have devoted regulator for current sharing. Instead sharing of load current occurs by means of sensing input voltage, output voltage and load current. This results in round-about duty ratio adjustment. The proposed scheme is useful in obtaining correct sharing of load current.

KEYWORDS: PV Array; PSLLCs; Parameter mismatches; Current sharing; Lag-Lead Compensator, FLC.

I. INTRODUCTION

Energy systems that exist have many destructive effects on human health and natural environment. Particularly carbon dioxide and other green house coming out of fossil fuel burning results in unexpected changes in the earth’s atmosphere [1-2]. The renewable energy sources are carbon-free and seem to be generally more supportive than fossil or nuclear fuels. Among various renewable energy sources, the photovoltaic (PV) power generation systems become a suitable and promising solution. Because PV system produces electric power without polluting environment and convert solar radiation into electricity [3-4]. PV electricity can be utilized for operating household appliances, telecommunication etc.

Solar cells operate on a principle of “photovoltaic effect” to generate electricity [5]. The cost of producing solar power is more. So it is essential to allow solar panels to function at their maximum power conditions. To track maximum power, maximum power point tracking algorithm (Perturb and observe method) is used [6-10].

PV power change based on the weather conditions and geographical location. In order to provide enough energy to load during power variations, a lead-acid battery is used to store energy when there is full radiation. Lead-acid battery supply power to load through converter during shortage of solar power [11-12]. In general DC-DC converters are used to supply power from battery to load. This paper proposes positive super lift Luo converter (PSLLC) to provide a regulated output to load. PSLLC is a DC-DC step-up boost converters, which was developed based on principle of voltage lift technique [13]. This paper analyses input parallel output parallel (IPOP) connected positive super lift Luo converters with solar array input for providing higher output current and to obtain a regulated output voltage to load. Connection of two converter modules in parallel may results in current inequality due to converter circuits with different parameters. To ensure equal output current sharing in presence of parameter mismatches, a new control scheme without a dedicated current controller is proposed. In the proposed scheme adjustment of duty ratio of converter modules depend on individual output currents, output voltage and input voltage of IPOP connected converters.

In [14] a control scheme is proposed for current sharing. Two loops were used, an output voltage loop and an inner current loop. The control scheme was implemented using DSP. The inner current loop needs a dedicated current controller and direct adjustment of duty ratio takes place. In [15] a three-loop control strategy, consisting of common output voltage regulation (OVR) loop, individual circulating current suppression (CCS) loops and individual inner current tracking (ICT) loops were used for current sharing. In this method increase in number of loops increases circuit complexity. Weicai et al. [16] proposed a reactive power balance current sharing method based on double closed-loop decoupling control and direct current control. The control scheme was implemented using PI controller. Hugues Renaudineau et al. [17] proposed new current-sharing technique on parallel DC-DC boost converters. Here output voltage and individual input currents are regulated through a two-loop control design based on flatness theory and sliding mode controllers.

Bashar Khasawneh et al. [18] proposed a new control technique to improve the performance of paralleled connected DC-DC converters. The control scheme was implemented using sliding mode controller, in which direct adjustment of duty ratio takes place. Sahiban et al. [19] implemented a control scheme using fuzzy sliding mode controller for current sharing in two parallel connected DC-DC converters. The control scheme was implemented in real time using dSPACE control board.

Thottuvilet et al. [20] presented a small-signal stability analysis of paralleled power converter systems. Here stable current sharing was implemented using combined performance of democratic and master current sharing schemes. This paper proposes equal sharing of load current in IPOP connected PSLLCs. In [14] to [20] current sharing takes place with a dedicated current controller and direct adjustment of duty ratio takes place. In this paper a new control scheme is proposed, which consists of voltage loop and current loop. The former loop helps to obtain a regulated output voltage using FLC. The later loop performs
current sharing without a dedicated current controller. Also the control scheme doesn’t adjust the duty ratio of individual converter modules directly. The adjustment of duty ratio depends on input voltage, output voltage and output currents of paralleled connected PSLLCs.

PV, VI and IV characteristics of PV cell are presented in section 2. Section 3 presents block diagram of proposed system. Section 4 presents the operation and mathematical model of PSLLC. Design of Lag-Lead compensator and Fuzzy Logic Controller for PSLLC are presented in section 5. Section 6 gives the simulation results. The conclusion is discussed in section 7.

2. PHOTOVOLTAIC SYSTEM

Photovoltaic technology works on the principle of converting solar energy into electrical energy. The fundamental element of a PV system is the solar cell. Solar cell helps in converting sunlight into electricity.

2.1. Modelling of PV Cell

Equivalent circuit of solar cell is shown in Fig. 1. Once solar radiation is incident on solar cell photocurrent (Iph) gets generated and flows to the output. Increase in load resistance results in increasing voltage across the diode. Hence small amount of current flows through the diode. If there is zero load resistance, the voltage drop is zero and hence entire current flows through the diode[21]. The mathematical equation use to express the current to load of a PV cell is given as

\[
l = I_p - I_s \left( \exp \left( \frac{q(V + R_s I)}{NKT} \right) - 1 \right) - \left( \frac{V + R_s I}{R_{sh}} \right)
\]

In this equation Iph is the photocurrent, Is is the reverse saturation current of the diode, q is the electron charge, V is the voltage across the diode, K is the Boltzmann's constant.

![Fig. 1. Equivalent circuit of a PV Cell](image)

Fig. 1. Equivalent circuit of a PV Cell

T is the junction temperature, N is the ideality factor of the diode, and Rs and Rsh are the series and shunt resistors of the cell, respectively. From above equation it is known that the characteristics of PV will be changed when solar illumination changes.

2.2. Maximum Power Point Tracker

For tracking maximum power, Perturb and Observe algorithm is preferred. It can be implemented easily. In this algorithm initially power from PV array is observed. If it is increasing, the operating point should be agitated in the same direction further. If there is decreasing in power of solar array, the agitation of operating voltage must be reversed [22]. Perturb and Observe algorithm tracks maximum power for varying environmental conditions.

![Fig. 2(a). P-V Characteristics Curve of PV Array](image)

Fig. 2(a). P-V Characteristics Curve of PV Array

![Fig. 2(b). I-V Characteristics Curve of PV Array](image)

Fig. 2(b). I-V Characteristics Curve of PV Array

3. PROPOSED BLOCK DIAGRAM AND CONTROL SCHEME

The block diagram of proposed system is shown in Fig. 3. The main blocks are solar array, buck-boost converter, MPPT controller, battery and IPOP connected PSLLCs which acts as a load regulator. Solar array provides a substantial proportion of energy to load. When the power of solar array is more than load requirement, solar array charges battery to ensure continuity of power [23]. In case if the power from solar array is insufficient, solar array and battery together supply the required energy to loads. During absence of radiation battery alone supplies energy to load. Buck-Boost converter acts as a solar regulator. The solar regulator control electricity flow from solar array to the battery and the load. The regulator helps in protecting battery from overcharging it. When power is delivered to load, the regulator helps to flow charge from solar array into the battery, the load or both. If there is full charge in battery, regulator prevents charge flow from solar array. Similarly if more charge is taken from battery to load, it is sensed by regulator. Regulator prevents charge flow from battery to load until enough charge is stored in battery. This helps to extend battery life time.

Battery used in the proposed system is lead acid battery. Thicker lead plates of lead acid battery make them tolerate deep discharge. The life span of lead acid battery increases with thicker the lead plates. The nominal voltage of battery is chosen as 12V.

In the proposed system IPOP connected PSLLCs act as a load regulator. The input and output of two PSLLCs are connected to ensure higher output current. Current inequality takes place if there is parameter mismatches.

The control scheme consists of voltage loop and a current controller [24]. The voltage loop generates a control signal (Iv). The difference between control signal (Iv) and sum of signals from input voltage (Vg) along with its gain Hv, output voltage (Vo) along with its gain Hv and output currents (Io) adjust the
When switch is closed the average values of inductor under mode 2 is shown in Fig. 5(b).

Under mode 2 the switch is closed. Circuit of PSLLC change with constant slopes during first sub interval.

PSSL C consists of an input supply voltage $V_{in}$ and output voltage $V_g$. The circuit parameters are capacitors $C_1$ and $C_2$, the inductor $L_1$, switch $S$, diodes $D_1$ and $D_2$ and the load resistance $R$. Considering that PSLLC operates in Continuous conduction mode (CCM), there are two different modes of operation based on switch closed and switch open. PSLLC circuit with switch open and closed is shown in Fig. 4 (a) and Fig. 4 (b) respectively.

4. SMALL SIGNAL MODELING OF PSLLC

The circuit diagram of PSLLC is shown in Fig. 4[25].

Fig. 4(a). Mode 1 Operation of PSLLC

Under mode 1 the averaged values of inductor voltage and capacitor currents are

$$v_L(t) = L \frac{di_L(t)}{dt} = <v_g(t)>_T$$  

$$i_{C_1}(t) = C_1 \frac{dv_1(t)}{dt} = <v_{in}(t)>_T - <i_{C_2}(t)>_T$$  

$$i_{C_2}(t) = C_2 \frac{dv_2(t)}{dt} = \frac{-<v_{o}(t)>_T}{R}$$  

Changes in inductor current and capacitor voltages when switch is closed are given by equations (6), (7) and (8).

4.1 Averaging inductor waveforms

Evaluation of equation (2) results in averaging of inductor voltage, (ie)

$$<v_L(t)>_{T_s} = \frac{1}{T_s} \int_{t}^{t+T_s} v_L(t)dt.$$  

Averaged inductor voltage under mode 1 and mode 2 are given by

$$<v_L(t)>_{T_s} = d(t) + v_o(t) + d''(t)$$  

Where $d''(t) = 1 - d(t)$. Right side of equation (10) indicates that there are no switching harmonics. From equation (6) the variation of inductor current with time is given by

$$L \frac{d}{dt} <i_L(t)>_{T_s} = d(t) + v_o(t) + d''(t)$$  

4.2 Averaging the capacitor waveforms

Averaging of equations 2, 3, 6 and 7 gives average current of capacitor $C_1$ (ie)

$$<i_{C_1}(t)>_{T_s} = <i_{C_1}(t)>_{T_s} - <i_{C_2}(t)>_{T_s} - <i_{in}(t)>_{T_s}$$  

Similarly the average current of capacitor $C_2$ from equation 2, 4, 6 and 8 is

$$<i_{C_2}(t)>_{T_s} = <i_{C_2}(t)>_{T_s} - <i_{o}(t)>_{T_s}$$  

Equations (12) and (13) indicate ac variations in the capacitor voltages.

4.3 The Average Input Current

Averaging of input Current is essential for modeling the dc component of converter input current. By means of this frequency variations at the input port of converter can be modeled.

From Fig. 5 (a) the input current of converter is

$$i_{g}(t) = <i_{C_1}(t)>_{T_s} + <i_{C_2}(t)>_{T_s}$$  

When switch is closed, the converter input current is

$$i_{g}(t) = <i_{C_1}(t)>_{T_s} + <i_{o}(t)>_{T_s}$$  

Average input current for one switching period is

$$<i_{g}(t)>_{T_s} = d(t) <i_{C_1}(t)>_{T_s} + <i_{C_2}(t)>_{T_s} + d''(t) <i_{o}(t)>_{T_s}$$  

$4.4$ Perturbation and Linearization

Averaging equation of quantities varying with time result in non linear system. Time domain and frequency domain techniques are not helpful for analyzing non linear systems. Hence it is important to perform linearization by building a small signal model.

Because of involvement of time varying quantities averaging equations are said to be non linear. Most of
the techniques of ac circuit analysis, such as the Laplace transforms and other frequency-domain methods are not useful for nonlinear systems. So it is essential to line arise by constructing a small signal model.

To develop a small signal model assume that input voltage \( v_g(t) \) and the duty cycle \( d(t) \) are equal to some given quiescent values \( V_g \) and \( D \), plus some superimposed small ac variations \( \bar{v}_g(t) \) and \( \bar{d}(t) \). Hence

\[
< v_g(t) > = V_g + \bar{v}_g(t).
\]
\[
d(t) = D + \bar{d}(t).
\]  

(17)

(18)

Assuming that the variation of ac component is small than the dc component the linearised form of non linear equations (2), (3) and (4) can be obtained.

The linearised equation for inductor is

\[
L \frac{d\bar{I}_L}{dt} = \bar{v}_L(t) + D(\bar{v}_1(t) - \bar{v}_2(t)) - \bar{d}(t)(V_1 - V_2).
\]  

(19)

Similarly the linearised capacitor equations are

\[
C_1 \frac{d\bar{I}_{C_1}}{dt} = -D\bar{I}_{C_1}(t) - \bar{d}(t)I_{L_1} + i_{i_1}(t).
\]
\[
C_2 \frac{d\bar{I}_{C_2}}{dt} = -\bar{v}_0(t) - \bar{d}(t)I_{L_0} + D'i_{i_0}(t).
\]  

(20)

(21)

Finally the linearised equation of the average input current is

\[
L\bar{I}_g(t) = D\left(\bar{I}_{C_1}(t) + \bar{I}_{C_2}(t)\right) + \bar{d}(t)(I_{L_1} + I_{C_1} - I_{C_2} - I_0) + D'\left(\bar{I}_{C_2}(t) + \bar{I}_{C_0}(t)\right).
\]  

(22)

Equation (19) explains the voltage around a loop where inductor is present. Small signal equivalent circuit of ac inductor loop equation is shown in Fig. 5.

Fig. 5. Circuit equivalent to the small-signal ac inductor loop equation

Current passing through a node is described by capacitor equations (20) and (21). Circuit equivalent to the small-signal ac capacitor node equations (20) and (21) is shown in Fig. 6.

Fig. 6. Circuit equivalent to the small-signal ac capacitor node equation

Equation (22) describes the small-signal ac current \( \bar{I}_g(t) \) flows through inductor due to the input voltage source \( \bar{v}_g(t) \). Equivalent circuit of small-signal ac input source current equation is shown in Figure 7.

Fig. 7. Circuit equivalent to the small-signal ac input source current equation

From Fig. 5, 6 and 7 the Small signal equivalent circuit of PSLLC is obtained which is shown in Fig. 8.

![Fig. 8. Small signal equivalent circuit of PSLLC](image)

Two independent ac inputs are present: the control input \( \bar{d}(s) \) and the line input \( \bar{v}_g(s) \). The variations of ac output voltage \( \bar{v}(s) \) is given as

\[
\bar{v}(s) = G_{vd}(s)\bar{d}(s) + G_{vg}(s)\bar{v}_g(s).
\]  

(23)

Line – to – output transfer function \( G_{vg}(s) \), is obtained by setting \( \bar{d} \) sources to zero. The equivalent circuit is shown in Figure 9.

![Fig. 9. Circuit to find line to output transfer function.](image)

From Fig. 9, the transfer function \( G_{vg}(s) \) is found using the voltage divider formula:

\[
G_{vg}(s) = \frac{\bar{v}(s)}{\bar{v}_g(s)} = \left(\frac{D}{D'}\right)\left(\frac{1}{1 + \frac{L_0}{R} + \frac{L_0(C_1 + C_2)}{D'2}}\right).
\]  

(24)

Control – to – output transfer function \( G_{vd}(s) \) is obtained by setting \( \bar{v}_g(s) \) sources to zero. The resultant circuit is shown in Fig. 10.

![Fig. 10. Circuit to find control to output transfer function.](image)

When current source of Fig. 10 is removed, the resultant circuit is shown in Fig. 11.

![Fig. 11. Circuit to find control to output transfer function, when current source is removed](image)

Circuit when voltage source of Fig. 10 is set to zero is shown in Fig. 12.
The transfer function $G_{eq}(s)$ from Fig. 12 is given by:

$$
G_{eq}(s) = \frac{\dot{E}_o(s)}{d(s)} = \frac{V_2 - V_2}{D'} \left[ \frac{1 + S^2 L / R Do}{1 + S^2 L / R Do} \right].
$$

Equation (26) gives the expression for control to output transfer function.

5. Design of Fuzzy Logic Controller and Compensators

The Fuzzy Logic Controller (FLC) helps in achieving good system performance by providing an adaptive control [26]. The controlling action of FLC depends on the values of fuzzy sets. FLC block diagram for controlling DC–DC converters is shown in Fig. 15.

![Fig. 15. Block diagram of FLC](image)

The three basic blocks of FLC are fuzzification, decision making and defuzzification. Fuzzification classifies input data into corresponding linguistic values or sets, decision making refers to inference of control action from rule base; converting fuzzified value into real value is defuzzification.

Degrees of membership of each input variable based on the membership functions are evaluated by means of fuzzifier. For two input variables two membership functions with five linguistic fuzzy subsets PB, PS, Z, NS and NB were created. FLC two input variables are error and change in error and its membership functions are shown in Fig. 16.

Index representation helps to create rule base of FLC. The linguistic labels representation of rule base for proposed system is shown in Table 1.

The fuzzy rules are generated in order to improve the converter performance based on the following criteria:

1. The change of control signal should be large if converter output is highly deviated from reference.
2. The change in control signal is small if converter output is closer to reference.
3. If converter output is nearer to reference value, the control signal continues to remain in same state to prevent overshoot.
4. If converter reference value is reached and even if change in output exists, the change in control signal is small, which supports to stops the output from moving away.
5. If the output of converter is above the reference, the sign of control signal generated is negative. The values of input and output variables are normalised. The result of inferred output is linguistic. Hence to achieve real value it is essential to perform defuzzification. The defuzzification method preferred here is centre of gravity.

<table>
<thead>
<tr>
<th>$\frac{e}{de}$</th>
<th>NB</th>
<th>NS</th>
<th>ZE</th>
<th>NS</th>
<th>PS</th>
<th>PB</th>
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<tbody>
<tr>
<td>NB</td>
<td>NB</td>
<td>NB</td>
<td>NB</td>
<td>NS</td>
<td>PS</td>
<td>PB</td>
</tr>
<tr>
<td>NS</td>
<td>NB</td>
<td>NB</td>
<td>ZE</td>
<td>NS</td>
<td>PS</td>
<td>PB</td>
</tr>
<tr>
<td>ZE</td>
<td>NS</td>
<td>NB</td>
<td>ZE</td>
<td>NS</td>
<td>PS</td>
<td>PB</td>
</tr>
<tr>
<td>PS</td>
<td>NS</td>
<td>NB</td>
<td>ZE</td>
<td>PS</td>
<td>PB</td>
<td>PB</td>
</tr>
<tr>
<td>PB</td>
<td>ZE</td>
<td>PS</td>
<td>PB</td>
<td>PB</td>
<td>PB</td>
<td>PB</td>
</tr>
</tbody>
</table>

![Fig. 16(a). Membership function for error, (b). Change in error and (c). Output for FLC.](image)

As in Fig.3 the voltage controller uses FLC. Fuzzy control of FLC for the chosen converter is developed using input membership functions error ‘$e(k)$’ and change in error $\Delta e(k)$ and are defined as:

$$
e(k) = V_{ref} - V_o,
$$

$$
\Delta e(k) = e(k) - e(k - 1).
$$

Where $V_{ref}$ is the reference voltage and $V_o$ is the actual output voltage of PSLLC at the $k_{th}$ sampling time. The output from FLC is the change in duty ratio $\Delta d$.

The output signal from FLC acts as a reference signal for current controller. Current controller make variation in duty cycle of respective converters based on the values of output currents, output voltage and input voltage to achieve equal sharing of load current between two IPB connected PSLLCs.

5. DESIGN OF COMPENSATORS

In general compensator is used to modify system performance of system in order to meet required specifications. Lead compensator helps to reduce transients and attenuates noise. Lag compensator improves steady state accuracy, but increase transients.

![Fig. 18. Open loop response of PSLLC](image)

Lag compensation reduce the effects of high frequency noise signals.

The characteristics of lead compensator and lag compensator get combined to get Lag-lead
compensator. In the proposed system from the open loop response of PSLLC, voltage compensator is designed. Fig. 18 gives the open loop response of PSLLC.

The designed voltage compensator from open loop response of PSLLC is shown in Table 2.

### Table 2. Voltage Compensator

| Parameter | Formula
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Lead</td>
<td>$1.4297e-4s + 0.29$</td>
</tr>
<tr>
<td>Lag</td>
<td>$0.0137s + 2.64$</td>
</tr>
<tr>
<td>Lag-lead</td>
<td>$2.28e - 6s^2 + 5.56e - 6s + 1$</td>
</tr>
</tbody>
</table>

### Results and Discussions

The parameters of PV module and PSLLC used for simulation are shown in Table 3 and Table 4 respectively.

### Table 3. BPX150 PV module specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak Power ($P_{pv}$)</td>
<td>80 W</td>
</tr>
<tr>
<td>Peak power voltage ($V_{pv}$)</td>
<td>16V</td>
</tr>
<tr>
<td>Current at peak power ($I_{pv}$)</td>
<td>5 A</td>
</tr>
<tr>
<td>Open circuit voltage ($V_{oc}$)</td>
<td>0.9 V</td>
</tr>
<tr>
<td>Short circuit current ($I_{sc}$)</td>
<td>5A</td>
</tr>
</tbody>
</table>

Charging and discharging of battery, the load voltage and current under irradiations are discussed in this section. The control scheme is implemented using Fuzzy and Lag-Lead compensators.

The testing of the system performance is done for startup transients, parameter mismatches and load variations.

Figure 19 shows simulation waveforms with $C_{11} = 30 \mu F$ and $C_{12} = 35 \mu F$.

### Table 4. Parameters of Parallel connected PSLLCs

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>$V_i$</td>
<td>12V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>$V_o$</td>
<td>36V</td>
</tr>
<tr>
<td>Inductor</td>
<td>$L_{1}, L_{2}$</td>
<td>100uH</td>
</tr>
<tr>
<td>Capacitors</td>
<td>$C_{11}, C_{12}$</td>
<td>30uF</td>
</tr>
<tr>
<td>$C_{21}, C_{22}$</td>
<td>30uF</td>
<td></td>
</tr>
<tr>
<td>Nominal switching frequency</td>
<td>$f_s$</td>
<td>100KHz</td>
</tr>
<tr>
<td>Load resistance</td>
<td>$R$</td>
<td>50</td>
</tr>
<tr>
<td>Range of duty ratio</td>
<td>$d$</td>
<td>0.3 to 0.9</td>
</tr>
</tbody>
</table>

Figure 19(a) shows the response of output voltage of IPOP connected PSLLCs for various solar radiations and for load resistance of $50 \Omega$. The response settles at 0.0125s and 0.022s for fuzzy and Lag-Lead compensator respectively. The peak overshoot is 38.5% for fuzzy and 36.5 % for lag-Lead compensator. The response has a peak time of 0.01s both for fuzzy and lag-Lead compensator.

Figure 19(b) shows the response of output current of IPOP connected PSLLCs for various solar radiations and for $R=50 \Omega$ with fuzzy and Lag-Lead compensator. It indicates that the output current of the paralleled modules has a little overshoot of 0.77% and 0.73% and a settling time of 0.0125s and 0.022s for fuzzy and lag-Lead compensator respectively.

Figure 19(c) shows the response of average output current of module 1 of IPOP connected PSLLCs for various solar radiations and for $50 \Omega$. It can be seen that the output current of module 1 has a slight overshoot of 0.385% and 0.365% and a settling time of 0.0125s and 0.022s for fuzzy and lag –lead compensator respectively.
Figure 19. Simulation waveforms of IPOP connected PSLLCs in start-up for various solar radiations and $R=50\Omega$ with $C_{11} = 30\mu F$ and $C_{12} = 35\mu F$

(a). Response of output voltage
(b). Response of output current
(c). Response of average output current1
(d). Response of average output current2

Figure 20. Simulation waveforms of IPOP connected PSLLCs for change in load resistance from $R=50\Omega$ to $R=40\Omega$ at $t=0.03\ s$ with $L_1 = 100\mu H$ and $L_2 = 102\mu H$

(a). Response of output voltage
(b). Response of output current
(c). Response of output current of module 1
(d). Response of output current of module 2

Figure 21. Simulation waveforms of IPOP connected PSLLCs for change in load resistance from $R=50\Omega$ to $R=40\Omega$ at $t=0.03\ s$ with $C_{11} = 30\mu F$ and $C_{22} = 35\mu F$

(a). Response of output voltage
(b). Response of output current
(c). Response of output current of module 1
(d). Response of output current of module 2
Figure 22. Simulation waveforms of IPOP connected PSLLCs for various values of load resistances $R=40\Omega, R=50\Omega$ and $R=60\Omega$ with $C_{11}=30\mu F$ and $C_{12}=35\mu F$.
(a) Response of output voltage (b). Response of output current (c). Response of output current of module 1 (d). Response of output current of module 2.

Figure 22(c) shows the response of the average output current of module 1 for different values of resistances with fuzzy logic controller. It can be seen that the response has a peak overshoot of 0.475%, 0.385% and 0.325% for 40 $\Omega$, 50 $\Omega$ and 60 $\Omega$ respectively and a settling time of 0.0125s.

Figure 22(d) shows the response of the average output current of module 2 for different values of resistances with fuzzy logic controller. It can be seen that the response has a peak overshoot of 0.475%, 0.385% and 0.325% for 40 $\Omega$, 50 $\Omega$ and 60 $\Omega$ respectively and a settling time of 0.0125s.

Figure 22(a),(b),(c) and (d) indicates that fuzzy logic controller works well for all values of load resistances.

Table 5. Performances of PSLLCs with FLC and Lag-Lead Compensator

<table>
<thead>
<tr>
<th>Line/Load Variation</th>
<th>FLC</th>
<th>Lag-Lead</th>
</tr>
</thead>
<tbody>
<tr>
<td>(0-1000)W/m$^2$</td>
<td>$I_0$</td>
<td>$I_1$</td>
</tr>
<tr>
<td>40 $\Omega$</td>
<td>36</td>
<td>0.9</td>
</tr>
<tr>
<td>50 $\Omega$</td>
<td>36</td>
<td>0.72</td>
</tr>
<tr>
<td>60 $\Omega$</td>
<td>36</td>
<td>0.6</td>
</tr>
</tbody>
</table>

Table 5 indicates that the voltage regulation and current distribution takes place correctly for lead, lag and lag-lead compensators for various values of line and load distributions.

7. CONCLUSION

This paper has proposed a new control scheme for current sharing in IPOP connected PSLLCs for standalone photovoltaic system. The proposed control scheme ensures equal sharing of load current without a dedicated current controller. To obtain a regulated output voltage FLC was used. The performance of FLC was compared with Lag-Lead compensator. The system has been proved to be effective in load voltage regulation using FLC and Lag-Lead compensator. Improvement in transient response is observed in Lag-Lead compensator. In FLC the steady state accuracy is better when compared to Lag-Lead compensator, but with increasing transients. Charging and discharging of batteries under irradiations were studied.

Several simulation results were presented to study the performances of FLC and Lag-Lead compensators and about charging and discharging of batteries. Simulation results show that FLC and Lag-Lead compensators maintain a regulated output voltage.
and proper current distribution under various line and load variations.

The proposed method is suitable for an efficient power supply for satellite communication, Uninterruptible power supplies etc.

REFERENCES: