LEAKAGE REDUCTION AND STABILITY IMPROVEMENT OF SRAM USING MULTIPLE THRESHOLD TECHNIQUE

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ABSTRACT—This paper focuses on the power dissipations and stability analysis of low power 12T MTCMOS SRAM cell. With continuous technology scaling, power dissipation has become biggest challenges of VLSI industry in designing of these high speed and low power devices. With projected large memory content of future systems on chip devices, it is important to consider the leakage current and stability in Static Random Access Memory structures. Memory has been the driving force behind the rapid development of CMOS technology. L1 Cache and L2 Cache are used by the central processing unit of a computer to reduce the average time to access data from the main memory. Cache memory has static random access memory. Multi-threshold CMOS (MTCMOS) is the most commonly used leakage power suppression technique in integrated circuits.

INDEX TERMS— MTCMOS SRAM, Multi-threshold, stability, low power SRAM.

I. INTRODUCTION

Multi-threshold voltage transistors are typically provided in advanced CMOS technologies to achieve higher performance with a limited power consumption budget. Low-Vth transistors are employed on the critical signal delay paths to enhance the speed of a circuit. Alternatively, high-Vth transistors are utilized on the noncritical signal delay paths to suppress the leakage power consumption of the circuit. A new leakage current reduction circuit called a “improved Self-controllable Voltage Level (SVL)” circuit is developed and included to reduce the leakage power of 9T SRAM. An AVL circuit is added to the SRAM cell for controlling the effective voltage across it. The AVL switch can be added either at the ground node (AVL(G)) or supply node (AVLS).

The threshold voltages of transistors can be dynamically adjusted by body bias to suppress the leakage power consumption of a circuit block. When the potential difference across the source-to-substrate p-n junction of a transistor is 0V, this transistor is in zero body biased. When a negative voltage is applied across the source-to-substrate p-n junction, a transistor is reverse body biased. In this paper a novel 12T MTCMOS SRAM cell is proposed. The threshold voltage of the SRAM architecture is designed using body bias technique. A charge recycling technique is used to minimize the leakage currents and static energy dissipation during the mode transitions.

Two voltage sources are used at the output nodes to reduce the swing voltages, resulting in reduction of dynamic power dissipation during switching activity. The paper is organized as follows: Section II discusses about the Leakage reduction techniques conventional SRAM cell, SVL (Self-Controllable Voltage Level) and AVL (Adaptive Voltage Level), Section III circuit design and working principle of the proposed novel 12-T MTCMOS SRAM cell. Section IV describes the detailed analysis of the power dissipation and static noise margin of the proposed SRAM cell.

ILCONVENTIONAL SRAM CELL AND THE LEAKAGE REDUCTION TECHNIQUES

A. CONVENTIONAL 9T SRAM CELL

Fig. 1 shows the circuit diagram of a conventional SRAM cell. Word line is used for enabling the access transistors Q7 and Q5 for write operation. BL and BLB lines are used to store the data and its compliment. For write operation one BL is high and the other bit line is on low condition. For writing “0”, BL is Low and BLB is high. Due to zero value at Q, the Q2 transistor is ON and Q1 is OFF. So the charge is stored at Q bar line. Similarly in the write “1” operation, BL is high due to this Q6 is ON and the charge is stored on the Q is discharged through the Q3-Q4 path and due to this low value on the Q, Q1 is ON and Q2 is OFF, so the charge is stored on the Q.

B. SELF-CONTROLLABLE VOLTAGE LEVEL TECHNIQUE

The SVL (Self controllable Voltage Level) circuit is shown in the Fig. 2. The basic idea is that when the SRAM cell is in active mode means, the CL is low. And there is no degradation in noise margin. During standby mode, CL is high and reduced supply voltage is given to SRAM cell. This reduces the leakage current and also reduces noise margin. The drawback of this technique is that it cannot able to reduce the gate leakage current.
C. ADAPTIVE VOLTAGE LEVEL

The AVL (Adaptive Voltage level) scheme reduces the sub-threshold leakage as well as gate leakage current. In this technique, an AVL circuit is added to the SRAM cell for controlling the effective voltage across it. The AVL switch can be added either at the ground node (AVLG) or supply node (AVLS). The AVLG circuit will provide 0V at ground node during the active mode and increased voltage during the standby mode. This scheme is similar to that of the diode footed cache design scheme for controlling the leakages in SRAM. In that, a diode is designed with high threshold transistor for raising the ground level in standby mode. The 10T SRAM cell with AVLG circuit is shown in the Fig. 3 and the 10T SRAM cell with AVLS circuit is shown in Fig. 4.

![Fig. 3 Adaptive Voltage level Ground Node](image)

![Fig. 4 Adaptive Voltage level Supply Node](image)

III. CIRCUIT DESIGN AND WORKING PRINCIPAL OF THE PROPOSED NOVEL 12-T MTCMOS SRAM CELL

This paper proposes novel 12T MTCMOS SRAM architecture to achieve low power and higher stability. In the proposed design two voltage sources V1 and V2 are connected to the BL and BLB, respectively. Two NMOS transistors Q8 and Q6 are used, one connected with the BL and the other with the BLB directly to switch ON and switch OFF the voltage sources during writing operations. The basic 4T SRAM cell is having LVT transistors. The two sleep transistors S1 and S2 used are of HVT type, while in sleep condition. This is basically MTCMOS technology. NMOS sleep transistor S1 connects node M (also called virtual ground node) to ground whereas the PMOS sleep transistor S2, connects node N (also called the virtual supply node) to supply Vdd. Sleep transistors while in sleep condition disconnect logic cells from the supply and/or ground to reduce the current leakages in the sleep mode. The LVT transmission gate TG is connected between the two nodes M and N for providing charge sharing. In the simulation, the sizes of the TG and the sleep transistors S1 and S2 are chosen larger than the sizes of the logic cell transistors (Q1, Q2, Q3, and Q4) to maintain some trade-off between increased static plus dynamic power dissipations and higher wake up time of TG. The effect of low threshold voltages of N and P transistors of TG on power dissipation is not considered in this work. The proposed design is illustrated in Fig. 5. Sleep transistor signal ST and Charge sharing control signal CS provide the switching activity control on sleep transistors and TG, respectively.

A. OPERATION OF SLEEP TRANSISTOR

Consider the configuration shown in Fig. 5. NMOS sleep transistor S1 connects the virtual ground node, i.e., node M in the Fig.5, to the actual ground, whereas the other PMOS sleep transistor S2 connects the virtual supply node i.e., node N in the Fig.5, to the actual Vdd supply. During the active period, both sleep transistors S1 and S2 are in the linear region and the voltage values of the virtual ground node M and virtual supply node N are equal to 0 and Vdd, respectively. During Write “1” operation with active-to-sleep transition of the sleep transistors S1 and S2, these are turned off, and since these are chosen to be high threshold devices, a very little sub-threshold leakage current is allowed to flow through them. Thus virtual nodes M and N are floating during the sleep time. Now, if the duration of the sleep period is sufficiently long, virtual ground node (M) will be charged up to some voltage value very close to Vdd by the leakage current flowing through T3 (with T1 ON during Write “1” operation). Similarly, if the duration of the sleep period is long enough, virtual supply node (N) will be discharged to some voltage value very close to 0 by the leakage current flowing through Q2 (with Q3 ON during Write “1” operation).

If the total capacitances in the virtual ground node M and virtual supply node N are denoted by CM and CN, respectively, it is observed that during the active-to-sleep transition, CM is charged up from 0 to very closely Vdd while CN is discharged from Vdd to very closely 0 for Write “1” operation. During Write “0” operation, when the sleep to-active transition edge arrives at the gates of the sleep transistors to turn them ON, the voltage of virtual ground node (M) starts to fall toward 0, whereas the voltage of virtual supply (N) starts to rise toward Vdd.

B. BODY BIAS EFFECT

The number of threshold voltages available in a CMOS technology is limited. Body bias is an extra knob to tune the threshold voltages of transistors in a bulk CMOS technology. When the potential difference across the source-to-substrate junction of a transistor is 0V, this transistor is zero body biased. When a negative voltage is applied across the source-to-substrate p-n junction, a transistor is reverse body biased. The threshold voltage Vth of a reverse body biased transistor is increased as compared to zero body bias. Alternatively, when a positive voltage is applied across the source-to-substrate p-n junction, a transistor is forward body biased. The threshold voltage Vth of a forward body biased transistor is decreased as compared to zero body bias. Therefore, reverse body bias can be applied to logic gates on the non-critical signal delay paths for leakage power

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reduction in both ACTIVE and SLEEP modes without degrading the performance of a circuit.

IV. THE POWER DISSIPATION AND STABILITY ANALYSIS RESULT

A. POWER DISSIPATION

Simulation has been done in 45nm CMOS environment. Cadence is used for power analysis and stability analysis of proposed MTCMOS SRAM. Power analysis on the SRAM circuit was done using various techniques. Multi threshold technique SRAM consumes less power compared to the other techniques. 12T MTCMOS SRAM cell has been proposed using body bias threshold tuning method.

<table>
<thead>
<tr>
<th>TECHNIQUE</th>
<th>Power Consumption (µW)</th>
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<tbody>
<tr>
<td>Conventional 9T SRAM</td>
<td>10,31830</td>
</tr>
<tr>
<td>9T SRAM Cell With Normal SVL Circuits</td>
<td>2.336827</td>
</tr>
<tr>
<td>9T SRAM Cell With Improved SVL Circuits</td>
<td>1.251365</td>
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<td>Adaptive Voltage Level Supply Node</td>
<td>0.1164346</td>
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<tr>
<td>Adaptive Voltage Level Ground Node</td>
<td>0.1883836</td>
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<tr>
<td>MTCMOS Technique</td>
<td>0.098766</td>
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B. STABILITY ANALYSIS

Normally stability of the SRAM bit cell measured by the Static Noise Margin (SNM). In this paper SRAM bit cells were analyzed using the butterfly Curve. Butterfly Curve gets information about both read stability, write stability at one simulation process.

READ STABILITY

The cell becomes less stable with lower supply voltage, increasing leakage currents and increasing variability, all resulting from technology scaling. The stability is usually defined by the static noise margin as the maximum value of DC noise voltage that can be tolerated by the SRAM cell without changing the stored bit. Locating the smallest square between the two largest ones delimited by the eyes of the butterfly curve determines graphically the SNM shown in Fig. 7.

During reads, WL and BL are held at VDD. Break the feedback from the cross-coupled inverters. The butterfly curve by overlapping the VTC with its inverse Read. SNM is the side of the largest square fitted in the butterfly curve.

WRITE STABILITY

Besides the read stability for the SRAM cell, a reasonable write-trip point is equally important to guarantee the write-ability of the cell without spending too much energy in pulling down the bit-line voltage to 0 V. The SRAM butterfly curve can also be used as alternative for the write-ability. Since, it gives indications on how difficult or easy it is to write the cell.
V. CONCLUSION

Stability is the major issue in high speed CMOS VLSI design. In this paper a novel low power 12T MTCMOS SRAM has been proposed which dissipates lesser dynamic power during write operation due to lesser swing voltage which is provided by the voltage sources V1 and V2. The proposed SRAM cell also dissipates less static power during mode transitions due to charge recycling. This simulation shows that the proposed cell dissipates lesser power and better stability, than the other existing SRAM cells. Although transistor count and area are increased in comparison to those of other SRAM cells but total low power dissipation and better stability can easily dominate over this drawback. This proposed 12T SRAM cell can be used to provide low power solution in high speed devices like laptops, mobile phones, programmable logic devices etc.

REFERENCES


